REMARKS

Claims 1-26 are pending. Claims 1 and 21 have been amended. Claims 9-20 have been withdrawn from further consideration. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Applicants note that the Examiner has acknowledged the Applicant's claim for priority under 35 U.S.C. § 119(a)-(d) based on the Japanese Application 371106. Applicants also note that the Examiner has indicated that the Japanese Application cannot be used as priority because the U.S. Application was allegedly filed more than twelve months after the Japanese Application. Applicants submit that the Japanese Application was filed on December 6, 2000 (not June 12, 2000 as indicated in the Office Action) and therefore, Applicants U.S. filing on November 27, 2001 was in fact within the required twelve months.

Claim Objections

Claims 1 and 21 were objected to for minor informalities. Applicants have amended claims 1 and 21 to correct these informalities. Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection.

Claim Rejections Under 35 U.S.C. § 103

A. Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423). Applicants respectfully traverse this rejection.

Claim 1 recites, in part, a semiconductor device which includes an element substrate including a semiconductor layer formed over a semiconductor substrate with a dielectric film interposed therebetween. Claim 1 further recites that the element substrate has a groove formed therein with a depth extending from a top surface of the semiconductor layer into the dielectric film, the groove is formed to have an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally as to expose a bottom surface of the semiconductor layer and such that the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer. As admitted by the Examiner, Lee fails to disclose that the semiconductor device includes a groove having an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally so a to expose a bottom surface of the semiconductor layer. The Examiner alleges that Malik teaches this feature.

Malik teaches (column 4, lines 20-30) that each of the trenches 30 have different widths and spacing. There is no disclosure in Malik that the trench is formed to have an increased width portion such that the bottom of the semiconductor layer is exposed and such that the width of the increased width portion is greater than that of the groove in the semiconductor layer. Accordingly, no combination of Lee and Malik teach or suggest that the groove is formed to have an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally as to expose a bottom surface of the semiconductor layer and such that the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer, as recited in claim 1.

Claim 2 is believed allowable for at least the reasons presented above with respect to claim 1 by virtue of its dependence upon claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

B. Claim 3 was rejected under 35 U.S.C. § 103(a) over Lee in view of Malik and Applicants' Admitted Prior Art. Applicants respectfully traverse this rejection.

Claim 3 is believed allowable for at least the reasons presented above with respect to claim 1 by virtue of its dependence upon claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

C. Claims 6-8 were rejected under 35 U.S.C. § 103(a) over Lee in view of Malik, Applicants' Admitted Prior Art, and Hieda et al. (U.S. Patent No. 5,508,541). Applicants respectfully traverse this rejection.

Claims 6-8 are believed allowable for at least the reasons presented above with respect to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

D. Claim 21 was rejected under 35 U.S.C. § 103(a) over Lee in view of Malik and Applicants' Admitted Prior Art. Applicants respectfully traverse this rejection.

Claim 21 recites, in part, a semiconductor device which includes an element substrate including a semiconductor layer formed over a semiconductor substrate with a dielectric film interposed therebetween. Claim 21 further recites that the element substrate has a groove formed therein with a depth extending from a top surface of the semiconductor layer into the dielectric film, the groove is formed to have an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally as to expose a bottom

surface of the semiconductor layer and such that the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer. As admitted by the Examiner, Lee fails to disclose that the semiconductor device includes a groove having an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally so a to expose a bottom surface of the semiconductor layer. The Examiner alleges that Malik teaches this feature.

Malik teaches (column 4, lines 20-30) that each of the trenches 30 have different widths and spacing. There is no disclosure in Malik that the trench is formed to have an increased width portion such that the bottom of the semiconductor layer is exposed and such that the width of the increased width portion is greater than that of the groove in the semiconductor layer. Accordingly, no combination of Lee, Malik and Applicants' Admitted Prior Art teach or suggest that the groove is formed to have an increased width portion in the dielectric film, the dielectric film of the increased width portion being receded laterally as to expose a bottom surface of the semiconductor layer and such that the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer, as recited in claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

E. Claims 24-26 were rejected under 35 U.S.C. § 103(a) over Lee in view of Malik, Applicants' Admitted Prior Art, and Hieda et al. (U.S. Patent No. 5,508,541). Applicants respectfully traverse this rejection.

Claims 24-26 are believed allowable for at least the reasons presented above with respect to claim 21 by virtue of their dependence upon claim 21. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Applicants appreciate the Examiner's indication that claims 4, 5, 22, and 23 contain allowable subject matter and would be allowable if rewritten in independent form. However, in view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 21 have been amended as follows:

1. (Twice Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being [insulatively] formed over a semiconductor substrate with a dielectric film interposed therebetween;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer;

an impurity diffusion source buried in said increased width portion of said groove to be contacted with said bottom surface of said semiconductor layer; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

21. (Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being [insulatively] formed over a semiconductor substrate with a dielectric film interposed therebetween;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate after penetration through said dielectric film, said groove being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer and such that the

width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer;

a trench capacitor formed under said dielectric film to have a storage electrode as half buried in said groove;

an impurity diffusion source buried in said increased width portion of said groove to serve as a buried strap, bottom surface and top surface of said impurity diffusion source being contacted with said storage electrode and said bottom surface of said semiconductor layer, respectively;

a cap insulation film formed in said groove to cover said impurity diffusion source; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode, said transistor constituting a DRAM cell with said trench capacitor.

End of Appendix